

INFORMATION DISCLOSURE STATEMENT

Applicant : Arena et al.
App. No : 10/800,417
Filed : March 11, 2004
For : SiGe RECTIFICATION PROCESS
Examiner : Unknown
Art Unit : 2812

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

March 11, 2005

(Date)


Andrew N. Merickel, Reg. No. 53,317

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:


Enclosed for filing in the above-identified application is an Information Disclosure Statement by Applicant (PTO/SB/08 equivalent) listing 40 references to be considered by the Examiner. Also enclosed are 21 foreign patent references and/or non-patent literature as listed on the Information Disclosure Statement.

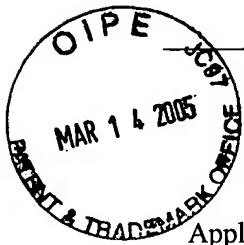
This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required. If a first Office Action on the merits was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: March 11, 2005

By: 
Andrew N. Merickel
Registration No. 53,317
Attorney of Record
Customer No. 20,995
(415) 954-4114



Please Direct All Correspondence to Customer Number **20995**

TRANSMITTAL LETTER
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Dear Sir:

Enclosed for filing in the above-identified application are:

- (X) An Information Disclosure Statement and PTO/SB/08 equivalent listing references for consideration:
 - (X) Listing 40 references.
 - (X) Enclosing 21 references.
- (X) The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Account No. 11-1410.
- (X) Return prepaid postcard.

Andrew N. Merickel
Registration No. 53,317
Attorney of Record
Customer No. 20,995
(415) 954-4114

MAR 14 2005

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Multiple sheets used when necessary)

SHEET 1 OF 3

Application No.	10/800,417
Filing Date	March 11, 2004
First Named Inventor	Chantal J. Arena
Art Unit	2812
Examiner	Unknown
Attorney Docket No.	ASMEX.446A

U.S. PATENT DOCUMENTS

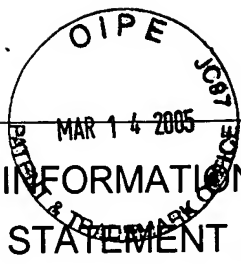
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	6,646,073	04/2003	Kondo	
	2	6,709,901	03/2004	Yamazaki, et al.	
	3	2002/0173130	11/2002	Pomerede, et al.	
	4	3,602,778	08/31/71	Ura, et al	
	5	3,720,877	03/13/73	Zarowin	
	6	3,729,645	04/24/73	Redington	
	7	3,737,739	06/05/73	Blakeslee, et al.	
	8	3,984,718	10/05/76	Fein, et al.	
	9	3,984,857	10/05/76	Mason	
	10	3,985,590	10/12/76	Mason	
	11	4,461,820	07/24/84	Shirai, et al.	
	12	4,656,013	04/07/87	Hiai, et al.	
	13	4,699,892	10/13/87	Suzuki	
	14	4,786,574	11/22/88	Shirai, et al.	
	15	4,803,186	02/07/89	Chen, et al.	
	16	4,857,270	08/15/89	Maruya, et al.	
	17	4,868,014	09/19/89	Kanai, et al.	
	18	4,983,274	01/08/91	Chen, et al.	
	19	5,037,775	08/06/91	Reisman	
	20	5,112,439	05/12/92	Reisman, et al.	
	21	5,281,274	01/25/94	Yoder	
	22	5,281,299	01/25/94	Escoffier, et al.	
	23	5,294,285	03/15/94	Kanai, et al.	
	24	5,316,958	05/31/94	Meyerson	
	25	5,366,554	11/22/94	Kanai, et al.	
	26	5,482,557	01/09/96	Kanai, et al.	
	27	5,576,247	11/19/96	Yano, et al.	
	28	5,646,073	07/08/97	Grider, et al.	
	29	5,667,586	09/16/97	Ek, et al.	

Examiner Signature

Date Considered

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Multiple sheets used when necessary)</i>	Application No.	10/800,417
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	First Named Inventor	Chantal J. Arena
	Art Unit	2812
SHEET 2 OF 3	Examiner	Unknown
	Attorney Docket No.	ASMEX.446A

U.S. PATENT DOCUMENTS

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	30	5,818,100	10/06/98	Grider, et al.	
	31	6,242,080 B1	06/05/01	Kondo	
	32	6,451,641 B1	09/17/02	Halliyal, et al.	
	33	6,515,219 B2	02/04/03	Kondo	
	34	2003/0010978 A1	01/16/03	Burden	
	35	2003/0111013 A1	06/19/03	Oosterlaken, et al.	
	36	2003/0157787	08/21/03	Murthy et al.	
	37	2003/0207127	11/06/03	Murthy et al.	
	38	2003/0235931	12/25/03	Wada et al.	
	39	2003/0230233	12/18/03	Fitzgerald et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T ¹
	40	JP 62017004	01/26/87	Japan		

NON PATENT LITERATURE DOCUMENTS

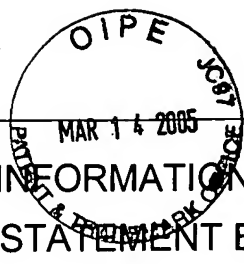
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ¹
	41	TAKAGI ET AL., "Device structure and electrical characteristics of strained-Si-on-insulator (strained-SOI) MOSFETs", Materials Science and Engineering B89 (2002), pp. 426-434	
	42	LIM ET AL., "Dry thermal oxidation of a graded SiGe layer", Applied Physics Letters, Vol. 79, No. 22, November 26, 2001, pp. 3606-3608	
	43	SUGIYAMA ET AL., "Fabrication of SiGe on Insulator Structure using Ge Condensation Technique", Third International Conference on SiGe (C) Epitaxy and Heterostructures (ICSI3), Santa Fe, NM, March 9-12, 2003, pp. 153-153	
	44	MIZUNO ET AL., "Advanced SOI p-MOSFETs with Strained-Si Channel on SiGe-on-Insulator Substrate Fabricated by SIMOX Technology", IEEE Transactions on Electron Devices, Vol. 48, No. 8, August 2001, pp. 1612-1618	
	45	MIZUNO ET AL., "Electron and Hole Mobility Enhancement in Strained-Si MOSFET's on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology", IEEE Electron Device Letters, Vol.21, No. 5, May 2000, pp. 230-232	
	46	MIZUNO ET AL., "Novel SOI p-Channel MOSFETs With Higher Strain in Si Channel Using Double SiGe Heterostructures", IEEE Transactions on Electron Devices, Vol 49, No. 1, January 2002, pp. 7-14	

Examiner Signature

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	Attorney Docket No.	ASMEX.446A

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ¹
	47	TSUTOMU TEZUKA, "Strained Si- and SiGe-MOSFETs on SiGe-on-insulator (SGOI) substrates", 2002 Japan Epitaxial Technology Symposium, "Advanced Substrate Engineering and Device Technology", February 27, 2002	
	48	TEZUKA ET AL., "Fabrication of strained Si on an ultrathin SiGe-on-insulator virtual substrate with a high-Ge fraction", Applied Physics Letters, Vol 79, No. 12, September 17, 2001, pp. 1798-1800	
	49	TEZUKA ET AL., "Fabrication of a strained is on sub-10-nm-thick SiGe-on-insulator virtual substrate", Materials Science and Engineering B89 (2002), pp. 360-363	
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	51	CANNON, D. ET AL., "Tensile strained epitaxial Ge films on Si(100) substrates with potential application in L-band telecommunications", Applied Physics Letters, Volume 84, Number 6, February 9, 2004, pp. 906-908.	
	52	COLACE, L. ET AL., "Efficient high-speed near-infrared Ge photodetectors integrated on Si substrates", Applied Physics Letters, Volume 76, Number 10, March 6, 2000, pp. 1231-1233.	
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	54	FAMA, S. ET AL., "High performance germanium-on-silicon detectors for optical communications", Applied Physics Letters, Volume 81, Number 4, July 22, 2002, pp. 586-588.	
	55	HULL, R., "Metastable strained layer configurations in the SiGe/Si system", (1999) EMIS Datareviews, Series No. 24: Properties of SiGe and SiGe:C, edited by Erich Kasper et al., INSPEC (2000), London, UK	
	56	ISHIKAWA, Y. ET AL., "Strain-induced band gap shrinkage in Ge grown on Si substrate", Applied Physics Letters, Volume 82, Number 12, March 31, 2003, pp. 2044-2046.	
	57	LEE ET AL., "Growth of strained Si and strained Ge heterostructures on relaxed Si _{1-x} Ge _x by ultrahigh vacuum chemical vapor deposition", J. Vac. Sci. Technol. B 22(1) (Jan/Feb 2004).	
	58	LI, Q. ET AL., "Selective growth of Ge on Si(100) through vias of SiO ₂ nanotemplate using solid source molecular beam epitaxy", Applied Physics Letters, Volume 83, Number 24, December 15, 2003, pp. 5032-5034.	
	59	LIU, J. ET AL., "Silicidation -induced band gap shrinkage in Ge epitaxial films on Si", Applied Physics Letters, Volume 84, Number 5, February 2, 2004, pp. 660-662.	
	60	MASINI, G. ET AL., "High-Performance p-i-n Ge on Si Photodetectors for the Near Infrared: From Model to Demonstration", IEEE Transactions of Electron Devices, Vol. 48, No. 6, June 2001, pp. 1092-1096.	
	61	SCHOLLHORN ET AL., "Coalescence of germanium islands on silicon", Thin Solid Films, Vol. 336 (1988), pp. 109-111.	

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